What is claimed is:

[Claim 1] A method of manufacturing a semiconductor package device, the method comprising:

a. providing a package substrate having a first coefficient of thermal expansion and at least one bonding pad on a surface of the package substrate;
b. forming an integrated circuit chip having electrical devices and having at least one coupling structure for electrically coupling the chip to the at least one bonding pad on the package substrate, the chip having a second coefficient of thermal expansion different than the first coefficient of thermal expansion;
c. removing a portion of a thickness of the chip that is free of the electrical devices sufficient to allow the chip to distort substantially with the package substrate during temperature changes despite the mismatch in their respective coefficients of thermal expansion; and
d. bonding the chip to the package substrate using the at least one coupling structure and the at least one bonding pad.

[Claim 2] A method according to claim 1, wherein the removing comprises removing about two-thirds of the thickness of the chip.

[Claim 3] A method according to claim 1, wherein the chip has an initial thickness of about 29 to 31 mils and the removing comprises removing until the chip has a final thickness of about 3-8 mils.

[Claim 4] A method according to claim 1, wherein the removing comprises grinding a portion of the thickness of the chip.

[Claim 5] A method according to claim 4, further comprising coupling a heat spreader to the ground surface of the chip.

[Claim 6] A method according to claim 1, wherein the at least one coupling structure comprises a metal.

[Claim 7] A method according to claim 1, wherein the at least one coupling structure is lead-free.

[Claim 8] A method according to claim 1, wherein the at least one coupling structure is a solder ball.

[Claim 9] A method according to claim 1, wherein forming an chip further comprises forming an inter-metal dielectric layer adjacent to a surface of the chip that is closest to the package substrate, and wherein the at least one coupling structure is located adjacent to the inter-metal dielectric layer.

[Claim 10] A method according to claim 1, further comprising separating the chip from a semiconductor wafer comprising a plurality of integrated circuit chips after the removing and before the bonding.

[Claim 11] A method according to claim 1, further comprising removing the portion of the thickness of the chip after the bonding.

[Claim 12] A method according to claim 1, further comprising separating the chip from a semiconductor wafer comprising a plurality of integrated circuit chips before the removing and before the bonding.

[Claim 13] A method according to claim 1, wherein forming a chip further comprises placing a dielectric encapsulant between the chip and the package substrate, the dielectric encapsulant substantially surrounding the at least one coupling structure and the at least one bonding pad.

[Claim 14] A method according to claim 1, wherein the package substrate is selected from the group consisting of glass, ceramic, a silicon-on-insulator, a polymer, silicon, silicon germanium, a single layer printed circuit board having conductive traces formed therein, and a multi-layer printed circuit board having conductive traces formed therein.

[Claim 15] A method according to claim 1, wherein the bonding comprises metallurgical bonding.

[Claim 16] A semiconductor package device, comprising:

a. a package substrate having a first coefficient of thermal expansion and at least one bonding pad on a surface of the package substrate; and
b. an integrated circuit chip formed from a semiconductor wafer, the chip comprising:
    i. electrical devices formed therein,
    ii. at least one coupling structure for bonding the chip to the at least one bonding pad on the package substrate,
    iii. a second coefficient of thermal expansion different than the first coefficient of thermal expansion, and
    iv. a final thickness less than a thickness of the semiconductor wafer, wherein the final thickness allows the chip to distort substantially with the package substrate during temperature changes despite the mismatch in their respective coefficients of thermal expansion.

[Claim 17] A semiconductor package device according to claim 16, wherein the final thickness is about one-third of the thickness of the semiconductor wafer.

[Claim 18] A semiconductor package device according to claim 16, wherein the thickness of the semiconductor wafer is about 29 to 31 mils and the final thickness of the chip is about 3-8 mils.

[Claim 19] A semiconductor package device according to claim 16, further comprising a heat spreader coupled to a surface of the chip free of electrical devices.

[Claim 20] A semiconductor package device according to claim 16, wherein the at least one coupling structure comprises a metal.

[Claim 21] A semiconductor package device according to claim 16, wherein the at least one coupling structure is lead-free.

[Claim 22] A semiconductor package device according to claim 16, wherein the at least one coupling structure is a solder ball.

[Claim 23] A semiconductor package device according to claim 16, further comprising an inter-metal dielectric layer adjacent to a surface of the chip that is closest to the package substrate, and wherein the at least one coupling structure is located adjacent to the inter-metal dielectric layer.

[Claim 24] A semiconductor package device according to claim 16, further comprising a dielectric encapsulant between the chip and the package substrate, the dielectric encapsulant substantially surrounding the at least one coupling structure and the at least one bonding pad.

[Claim 25] A semiconductor package device according to claim 16, wherein the package substrate is selected from the group consisting of glass, ceramic, a silicon-on-insulator, a polymer, silicon, silicon germanium, a single layer printed circuit board having conductive traces formed therein, and a multi-layer printed circuit board having conductive traces formed therein.

[Claim 26] A semiconductor package device according to claim 16, wherein the chip comprises at least one coupling structure for metallurgically bonding the chip to the at least one bonding pad on the package substrate.